AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listing, of claims in the specification:

Claims 1-17 (Cancelled)

18. (Currently Amended) A memory device comprising:

a muxing device; and

at least one cluster device coupled to said muxing device, wherein said at least one cluster device is a self-timed local element interfacing with at least said muxing device.

19. (Previously Presented) The memory device of Claim 18, wherein said cluster device is adapted to sink a tail current of at least one local sense amp contained in said cluster device.

20. (Previously presented) The memory device of Claim 18, further comprising a plurality of local cluster devices having at least one common local wordline coupling all said plurality of cluster devices in a block.

21. (Previously Presented) The memory device of Claim 18, wherein said cluster device comprises at least one sense amp adapted to be activated by a global cluster line.

22-42. (Cancelled)

43. (Previously presented) The memory device of Claim 18, wherein said at least one cluster device comprises an array of local sense amplifiers.

44. (Previously presented) The memory device of Claim 43 wherein said array of local sense amplifiers comprises four pairs of bitline multiplixers.

45. (Previously presented) The memory device of Claim 44 wherein each bitline multiplixer connects at least one bitline pair to a global bitline.

46. (Cancelled)

47. (Previously presented) The memory device of Claim 20 wherein at least one of said plurality of cluster devices comprises an array of local sense amplifiers.

48. (Previously presented) The memory device of Claim 47, wherein at least one of said plurality of cluster devices is adapted to sink a tail current of all said local sense amplifiers contained in said at least one cluster device.

49. (Previously presented) The memory device of Claim 18 comprising at least one global cluster line and at least one local cluster line.

50. (Previously presented) The memory device of Claim 49 wherein at least one local cluster line is coupled to at least one local sense amplifier in said at least one cluster device.

51. (Previously presented) A memory device comprising:

a plurality of muxing devices;

a plurality of cluster devices interfacing with at least one of said plurality of muxing devices; and

at least one common local wordline coupling said plurality of cluster devices in a block.

52. (Previously presented) The memory device of Claim 51, wherein at least one of said plurality of cluster devices is adapted to sink a tail current of at least one local sense amplifier contained in said at least one of said plurality of cluster devices.

53. (Previously presented) The memory device of Claim 51, wherein each of said plurality of cluster devices comprises at least one sense amplifier adapted to be activated by a global cluster line.

54. (Previously presented) The memory device of Claim 51, wherein at least one of said plurality of cluster devices comprises an array of local sense amplifiers.

55. (Previously presented) The memory device of Claim 54 wherein said array of local sense amplifiers comprises four pairs of bitline multiplixers.

56. (Previously presented) The memory device of Claim 55 wherein each bitline multiplixer connects at least one bitline pair to a global bitline.

57. (Previously presented) The memory device of Claim 56, wherein at least one of said plurality of cluster devices comprises a self-timed local element interfacing with at least one of said plurality of muxing devices.

58. (Previously presented) A method of performing at least one of a read and write operation in a memory device comprising:

activating at least one cluster device coupled to at least one muxing device in the memory device; and

firing at least one sense amplifier in said at least one cluster device.

59. (Previously presented) The method of Claim 58 comprising activating at least one global cluster line prior to the at least one of a read and write operation.

60. (Previously presented) The method of Claim 59 comprising using at external interface to activate said global cluster line.

61. (Previously presented) The method of Claim 58 comprising sinking a tail current of at least one local sense amp contained in said cluster device.

62. (Previously presented) The method of Claim 58 comprising firing a plurality of sense amplifiers in at least one of said plurality of cluster devices.

63. (New) A memory device comprising:

a muxing device; and

at least one cluster device coupled to said muxing device and adapted to sink a tail current of at least one local sense amplifier contained in said cluster device.

64. (New) The memory device of Claim 63, further comprising a plurality of local cluster devices having at least one common local wordline coupling all said plurality of cluster devices in a block.

65. (New) The memory device of Claim 63, wherein said at least one cluster device comprises at least one sense amplifier adapted to be activated by a global cluster line.

66. (New) The memory device of Claim 63, wherein said at least one cluster device comprises an array of local sense amplifiers.

67. (New) The memory device of Claim 66 wherein said array of local sense amplifiers comprises four pairs of bitline multiplixers.

68. (New) The memory device of Claim 67 wherein each bitline multiplixer connects at least one bitline pair to a global bitline.

69. (New) The memory device of Claim 64 wherein at least one of said plurality of cluster devices comprises an array of local sense amplifiers.

70. (New) The memory device of Claim 63 comprising at least one global cluster line and at least one local cluster line.

71. (New) The memory device of Claim 70 wherein said at least one local cluster line is coupled to said at least one local sense amplifier in said at least one cluster device.

72. (New) A memory device comprising:

a muxing device; and

a plurality of local cluster devices having at least one common local wordline coupling all said plurality of clusters devices in a block, at least one of said plurality of local cluster devices coupled to said muxing device.

73. (New) The memory device of Claim 72, wherein at least one of said plurality of local cluster devices comprises at least one sense amp adapted to be activated by a global cluster line.

74. (New) The memory device of Claim 72, wherein at least one of said plurality of local cluster devices comprises an array of local sense amplifiers.

75. (New) The memory device of Claim 74 wherein said array of local sense amplifiers comprises four pairs of bitline multiplixers.

76. (New) The memory device of Claim 75 wherein each bitline multiplixer connects at least one bitline pair to a global bitline.

77. (New) The memory device of Claim 72, wherein at least one of said plurality of cluster devices is adapted to sink a tail current of all said local sense amplifiers contained in at least one of said plurality of local cluster devices.

78. (New) The memory device of Claim 72 comprising at least one global cluster line and at least one local cluster line.

79. (New) The memory device of Claim 78 wherein said at least one local cluster line is coupled to at least one local sense amplifier in at least one of said plurality of local cluster devices.

80. (New) A memory device comprising:

a muxing device; and

at least one cluster device comprising at least one sense amplifier adapted to be activated by a global cluster line, said at least one cluster device coupled to said muxing device.

81. (New) The memory device of Claim 80, wherein said at least one cluster device comprises an array of local sense amplifiers.

82. (New) The memory device of Claim 81 wherein said array of local sense amplifiers comprises four pairs of bitline multiplixers.

83. (New) The memory device of Claim 82 wherein each bitline multiplixer connects at least one bitline pair to a global bitline.

84. (New) The memory device of Claim 80 comprising at least one local cluster line.

85. (New) The memory device of Claim 84 wherein said at least one local cluster line is coupled to said local sense amplifier.

86. (New) A memory device comprising:

a muxing device;

at least one global cluster line;

at least one local cluster line; and

at least one cluster device coupled to said muxing device.

87. (New) The memory device of Claim 86 wherein said at least one local cluster line is coupled to said at least one local sense amplifier in said at least one cluster device.